CLAIMS

1. A semiconductor memory device comprising:

a semiconductor substrate;

a memory cell array, disposed on the semiconductor substrate, having plural memory cells, word lines and data lines for selecting the memory cells; and

a peripheral circuit disposed on the semiconductor substrate;

wherein the memory cell has a multi-layer of a conductive layer, an insulating layer and plural semiconductor layers containing impurities, and a potential can be applied to the insulating layer that enables the movement of carriers by way of the multi-layer.

2. A semiconductor memory device comprising:

a semiconductor substrate;

a memory cell array, disposed on the semiconductor substrate, having plural memory cells, word lines and data lines for selecting the memory cells; and

a peripheral circuit disposed on the semiconductor substrate;

wherein the memory cell has a multi-layer of a conductive layer, an insulating layer and plural semiconductor layers containing impurities, and the multi-layer of the memory cell has bistable characteristics for the resistance

value.

3. A semiconductor memory device comprising:

a semiconductor substrate;

a memory cell array, disposed on the semiconductor substrate, having plural memory cells, word lines and data lines for selecting the memory cells; and

a peripheral circuit, disposed on the semiconductor substrate, which is constituted with plural insulated gate field effect transistors (MISFET) on the periphery of the memory cell array;

wherein the memory cell has a multi-layer of a conductive layer, an insulating layer that enables the tunneling effect and plural semiconductor layers containing impurities, and the semiconductor layers containing impurities are present in the semiconductor substrate.

4. A semiconductor memory device as defined in claim 1, wherein the plural semiconductor layers containing impurities constituting the memory cell have two semiconductor layers of different p-type and n-type conduction.

5. A semiconductor memory device as defined in claim 4, wherein a position of junction formed of the two semiconductor layers of different p-type and n-type conduction of the memory cell is shallower than the depth of a device isolation region formed in the semiconductor substrate.

6. A semiconductor memory device as defined in claim 4,

wherein a position of a PN junction of the memory cell is shallower than the depth of 0.3 μm from the surface of the semiconductor substrate.

7. A semiconductor memory device as defined in claim 4, wherein at least one of the plural semiconductor layers containing impurities of the memory cell has a impurity concentration that is higher in the inside of the semiconductor substrate than on the surface of the semiconductor substrate.

8. A semiconductor memory device as defined in any one of claims 4 to 7, wherein an impurity concentration of the layer present in contact with the surface of the semiconductor substrate among the plural semiconductor layers containing impurities for forming the memory cell is 1×10^{17} cm^{-3} or less on the surface of the semiconductor substrate.

9. A semiconductor memory device as defined in claim 4, wherein a maximum impurity concentration of a layer present in contact with the surface of the semiconductor substrate among the plural semiconductor layers containing impurities for forming the memory cell is 1×10^{17} cm^{-3} or more.

10. A semiconductor memory device as defined in claim 4, wherein a maximum impurity concentration of the layer present in the inside of the semiconductor substrate among the plural semiconductor layers containing impurities for forming the memory cell is 1×10^{17} cm^{-3} or more.

11. A semiconductor memory device as defined claim 4, wherein a position of PN junction of the memory cell is at a place deeper than a position at which an impurity concentration is maximum of a layer present in contact with the surface of the semiconductor substrate among the plural semiconductor layers containing impurities for forming the memory cell.

12. A semiconductor memory device as defined in claim 1, wherein the plural semiconductor layers containing impurities of the memory cell comprise two P-type layers putting an N-type layer therebetween, or two N-type layers putting a P-type layer therebetween.

13. A semiconductor memory device wherein which two P-type layers and an N-type layer present apart from the surface of the semiconductor substrate among the three semiconductor layers containing impurities of the memory cell satisfy the conditions as defined in claim 5.

14. A semiconductor memory device as defined in claim 3, wherein the conductive layer of the memory cell is a conductive layer connected to a gate electrode of an insulate gate field effect transistor in the peripheral circuit.

15. A semiconductor memory device as defined in claim 3, wherein the conductive layer of the memory cell comprises a multi-layer containing N-type or P-type polycrystal silicon.

16. A semiconductor memory device as defined in claim 3,

wherein the insulating layer of the memory cell is an insulating layer connected with an insulating layer of an insulated gate field effect transistor in the peripheral circuit.

17. A semiconductor memory device as defined in claim 1, wherein the insulating layer of the memory cell is a multi-layer of insulating layers having different band gaps.

18. A semiconductor memory device as defined in claim 17, wherein the insulating layer of the memory cell comprises a multi-layer of a silicon oxide layer and a silicon nitride layer and the silicon oxide layer is present in contact with a P-type semiconductor layer formed in a silicon substrate.

19. A semiconductor memory device as defined in claim 1, wherein at least one of plural semiconductor layers containing the impurities of the memory cell is present extending in a direction perpendicular to the word line in the semiconductor substrate.

20. A semiconductor memory device as defined in claim 1, wherein the layer in contact with the insulating layer for forming the memory cell among the plural semiconductor layers containing the impurities of the memory cell is present being separated on every memory cells.

21. A semiconductor memory device as defined in claim 1, wherein a conductive plug is electrically connected to a layer formed in the lowest portion among the plural semiconductor

layers containing impurities of the memory cell.

22. A semiconductor memory device as defined in claim 1, wherein a layer formed at the lowest portion among plural semiconductor layers containing impurities of the memory cell is electrically connected with a conductive layer extending in a direction perpendicular to the word lines in a planer arrangement.

23. A semiconductor memory device as defined in claim 1, wherein a layer present extending in a direction perpendicular to the word line in the planer arrangement among the plural semiconductor layers containing the impurities of the memory cell is electrically connected with one of diffusion layers of the insulated gate field effect transistor formed in the semiconductor substrate and connected electrically with the conductive layer extending in the direction perpendicular to the word line in the planer arrangement for the other of the diffusion layers of the insulated gate field effect transistor.

24. A semiconductor memory device including plural memory arrays each comprising:

plural word lines;

plural data lines arranged so as to intersect the plural word lines in a planer arrangement;

plural memory cells which are disposed each at a desired intersection between the plural word lines and the plural data lines and each connected to the corresponding word

line and corresponding data line;

a common data line disposed in common with the plural data lines; and

plural signal transmission means having a switching function for connecting the common data line to the plural data lines respectively;

wherein the memory cell has a multi-layer of a conductive layer, an insulating layer and a plural semiconductor layers containing impurities and a potential can be applied to the insulating layer that enables movement of the carriers by way of the multi-layer.

25. A semiconductor memory device including plural memory arrays each comprising:

plural word lines;

plural data lines arranged so as to intersect the plural word lines in a planer arrangement;

plural memory cells which are disposed each at a desired intersection between the plural word lines and the plural data lines and each connected to the corresponding word line and corresponding data line, a common data line disposed in common with the plural data lines; and

plural signal transmission means having a switching function for connecting the common data line to the plural data lines respectively;

wherein the memory cell has a multi-layer of a

conductive layer, an insulating layer and a plural semiconductor layers containing impurities and the multi-layer of the memory cell has a bistable characteristic of a resistance value.

26. A semiconductor memory device including plural memory arrays each comprising;

plural word lines;

plural data lines arranged so as to intersect the plural word lines in a planer arrangement;

plural memory cells which are disposed each at a desired intersection between the plural word lines and the plural data lines and each connected to the corresponding word line and corresponding data line;

a common data line disposed in common with the plural data lines; and

plural signal transmission means having a switching function for connecting the common data line to the plural data lines respectively;

wherein the memory cell has a multi-layer of a conductive layer, an insulating layer enabling a tunnel effect and a plural semiconductor layers containing impurities, and the plural semiconductor layers containing the impurities are present in the semiconductor substrate.

27. A semiconductor memory device as defined in claim 1, wherein at least the memory cell is formed on an On SOI

substrate.

28. A semiconductor memory device as defined in claim 1, wherein plural bit lines have one sense amplifier in common in the memory cell array region.

29. A semiconductor device wherein a bistable diode is configured to have a region included in a semiconductor substrate.

30. A semiconductor memory device wherein at least a portion of a memory device is disposed in the semiconductor substrate and a memory capacity is 256 Mbits or more.

31. A method of manufacturing a semiconductor memory device comprising:

a step of forming a device isolation region for electrically isolating devices in a semiconductor substrate;

a step of forming an impurity diffusion layer in the substrate by implantation of ions at high energy in a memory cell array region and then forming an insulating layer on the surface of the substrate;

a step of forming a word electrode in the memory cell array region and a gate electrode of an insulated gate field effect transistor in a peripheral circuit region;

a step of etching a silicon substrate using a region covering the word electrode as at least an area corresponding to a mask, and thereby isolating the memory array for every cells;

a step of depositing an interlayer insulating layer, then opening a contact hole and burying a conductive body into the contact; and

a step of forming a bit line in the memory cell array region and a local interconnect layer in the peripheral circuit region.